REMARKS/ARGUMENTS

1.) Claim Amendments

Claims 1, 2, 4-12, 14-18, and 20-23 are pending in the application. Favorable reconsideration of the application is respectfully requested in view of the following remarks.

2.) Claim Rejections – 35 U.S.C. § 103(a)

On Page 2 of the Office Action, the Examiner rejected claims 1-2, 4-5, 7-12, 14, 17-18, 20-21, and 23 under 35 U.S.C. § 103(a) as being unpatentable over Chatterjee et al. (US 5,634,046) in view of Wollan, et al. (US 5,854,939). The Applicant respectfully traverses this rejection.

As noted in Applicant's previous response, the Applicant's invention provides a dedicated direct path between ***the memory*** and ***the special-purpose register*** to allow transfer of memory address calculation in parallel with other data being transferred to and/or from the general register files. As discussed in the previous response, Chatterjee does not teach or suggest this feature. The Examiner has responded by changing the rejection to a § 103 rejection and stating this feature is shown *in* Wollan. In particular, the Examiner cites FIGS. 1 and 6, and states there is a dedicated direct interface between the stack pointer and the SRAM.

However, a direct interface between the stack pointer and the memory (SRAM) is not what is being claimed by the Application. The Applicant's claims recite a dedicated direct path between ***the memory*** and ***the special-purpose register***. FIGS. 1 and 6 of Wollen clearly do not show a dedicated direct path between the register file and the SRAM memory. Instead, the register file and the SRAM are connected through the 8-bit data bus 12, which also carries data to every other component in the microprocessor. The data bus is utilized even if going through the stack pointer. Thus, the interface between the SRAM and the register file is not a dedicated direct path.

Since neither Chatterjee nor Wollen teach or suggest a dedicated direct path between the memory and the special-purpose register, a prima facie case of

obviousness has not been established. Therefore, the withdrawal of the rejection and the allowance of independent claims 1, 15, and 17 are respectfully requested.

Claims 2, 4-5, 7-12, 14, and 23 depend from base claim 1. Claims 18, 20, and 21 depend from base claim 17. Therefore, the allowance of claims 2, 4-5, 7-12, 14, 18, 20-21, and 23 is respectfully requested.

On Page 25 of the Office Action, the Examiner rejected claims 15-16 and 22 under 35 U.S.C. § 103(a) as being unpatentable over Chatterjee in view of Aikawa, et al. (US 5,371,865). The Applicant respectfully traverses this rejection.

Independent claim 15 includes, among others, the following limitations:

> a dedicated special-purpose register file separate from other general register files of the computer system and adapted solely for holding memory access information received from said dedicated cache over a first dedicated interface;
>
> wherein said first dedicated interface includes a dedicated direct path between said special-purpose register file and the dedicated cache for loading said special-purpose access register file from the dedicated cache;

As noted in the Applicant's previous response, Chatterjee fails to disclose a dedicated special-purpose register file separate from other general register files of the computer system and adapted solely for holding memory access information. In fact, Chatterjee clearly teaches a register set that includes both special-purpose and general registers. Chatterjee also fails to disclose one dedicated interface having a dedicated direct path between the special-purpose register file and the dedicated cache for loading the special-purpose access register file from the dedicated cache.

The Examiner cites Aikawa's FIG. 4A and states the instruction register 43 corresponds to the claimed special-purpose register file. The Examiner then equates the "instruction" line between the instruction register 43 and the instruction cache memory 41 with the claimed dedicated direct path between the special-purpose register file and the dedicated cache. These comparisons are both clearly wrong. An instruction register holds *instructions*, not memory access information. A thorough review of Aikawa does not reveal any special-purpose register file. Thus, like

Chatterjee, Aikawa clearly does not disclose a dedicated special-purpose register file separate from other general register files of the computer system and adapted solely for holding memory access information received from the dedicated cache over a first dedicated interface. Since Aikawa does not disclose such a dedicated special-purpose register file, a dedicated interface having a dedicated direct path between the special-purpose register file and the dedicated cache cannot be disclosed or suggested.

Since neither Chatterjee nor Aikawa teach or suggest a dedicated special-purpose register file as claimed, or a dedicated direct path between the special-purpose register and the dedicated cache, a prima facie case of obviousness has not been established. Therefore, the withdrawal of the rejection and the allowance of independent claim 15 are respectfully requested.

Claim 16 depends from base claim 15 and recites further limitations in combination with the novel elements of claim 15. Therefore, the allowance of claim 16 is respectfully requested.

Claim 22 depends from base claim 17 and recites further limitations in combination with the novel elements of claim 17. Claim 17 also recites a dedicated special-purpose register file separate from other general register files of the computer system and adapted solely for holding memory access information, and a dedicated interface with a memory. As noted, these limitations are not taught or suggested by Chatterjee or Aikawa. Therefore, the allowance of claim 22 is respectfully requested.

On Page 33 of the Office Action, the Examiner rejected claim 6 under 35 U.S.C. § 103(a) as being unpatentable over Chatterjee et al. (US 5,634,046) and in view of Wollan et al. (US 5,854,939) and further in view of Aikawa, et al. (US 5,371,865). The Applicant respectfully traverses this rejection.

Claim 6 depends from base claim 1 and recites further limitations in combination with the novel elements of claim 1. As noted above, Chatterjee, Wollan, and Aikawa all fail to teach or suggest a dedicated special-purpose register file separate from other general register files of the computer system and adapted solely for holding memory address calculation information received from memory. By necessity, these references also fail to teach or suggest a dedicated direct path between the special-purpose

register and the dedicated cache. Therefore, the allowance of claim 6 is respectfully requested.

3.) Prior Art Not Relied Upon

On page 35 of the Office Action, the Examiner stated that the prior art made of record and not relied upon is considered pertinent to the Applicants' disclosure. However, Applicant's reading of these references has revealed no teaching or suggestion of a dedicated special-purpose register file separate from other general register files of the computer system and adapted solely for holding memory address calculation information received from memory, and a dedicated direct path between the special-purpose register and the dedicated cache, as claimed by the Applicant.

4.) Conclusion

In view of the foregoing remarks, the Applicants believe all of the claims currently pending in the Application to be in condition for allowance. The Applicants, therefore, respectfully request that the Examiner withdraw all rejections and issue a Notice of Allowance for claims 1, 2, 4-12, 14-18, and 20-23.

The Applicants request a telephonic interview if the Examiner has any questions or requires any additional information that would expedite the prosecution of the Application.

Respectfully submitted,

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